



**Title of Investigation:**

Wavefront Sensing via High Speed DSP (Digital-Signal-Processor)

**Principal Investigator:**

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**Other In-house Members of Team:**

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**Other External Collaborators:**

N/A

**Initiation Year:**

FY 2004

**Aggregate Amount of Funding Authorized in FY 2004 and Earlier Years:**

N/A

**FY 2004 Authorized Funding:**

\$15,300

**Actual or Expected Expenditure of FY 2004 Funding: Instruments, Lab Equipment, and Cabling: \$10K; Software: \$3K; Conference, Publication Costs, Ref Materials:**

\$2K

**Status of Investigation at End of FY 2004:**

As a result of the DDF 2004 award, an additional funding source was obtained in the amount of \$75K in 2004 to build a full 64 processor DSP unit. The DSP unit is operational and currently used for project support both internal to GSFC (SPOT IRAD 2004 and 2005) as well as external to the Dept of Defense (AFRL).

**Expected Completion Date:**

January 2005.

**Purpose of Investigation:**

Light-weighted and segmented primary mirror systems require active optical control to maintain mirror positioning and figure to within nanometer tolerances. An image-based wavefront sensor offers a simple solution that differs from conventional wavefront sensing approaches (e.g., Shack-Hartmann, shearing interferometry) in that complicated optical hardware is replaced by a computational approach where the science camera itself serves as the wavefront sensor. Current state-of-the-art techniques rely on post-processing to return an estimate of the aberrated optical

wavefront with accuracies to the nanometer level. But the lag times between wavefront sensing, and then control, which are characteristic of the post-processing approach, are often prohibitive for missions requiring near-real-time optical monitoring and correction. Typical lag times to return wavefront information are on the order of 10 minutes to several hours for the image-based approach.

Therefore, the purpose of this investigation is to accelerate the algorithms used for image-based wavefront sensing. The image-based wavefront sensing algorithm is very computational intensive in terms of floating point performance. Therefore, a special purpose computing architecture has been developed to accelerate the performance by better than two orders of magnitude.

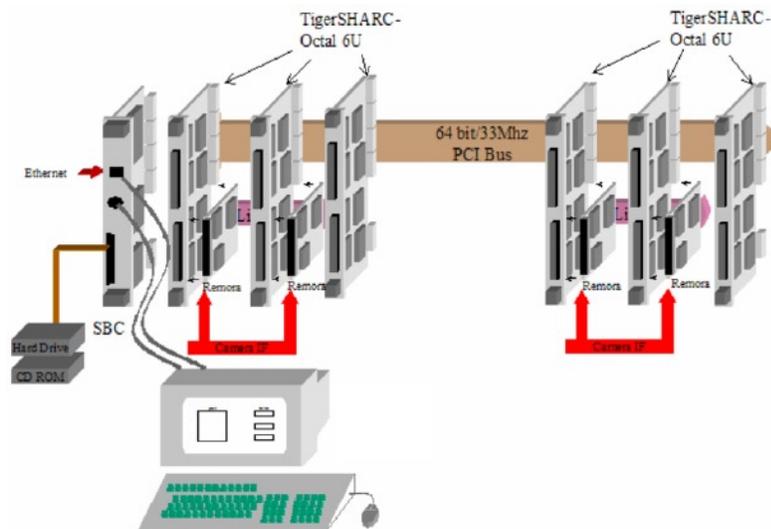
**FY 2004 Accomplishments:**

A high-speed computational architecture has been successfully developed for image-based wavefront sensing. Using this architecture, our wavefront sensing algorithm has been accelerated by a factor of 400. For example, using a desktop computer on a JWST (James Webb Space Telescope) type data set, the wavefront sensing computation normally takes about 8 minutes, but while using our high-speed wavefront sensing architecture, this calculation time has been reduced to approximately 1 second.

The computational hardware is based on a digital signal processor (DSP), specifically the Analog Devices TigerSharc TS-101. While numerous options exist for computational hardware between desktop processors to field programmable gate arrays (FPGA), the DSP provides the best balance between speed and modularity. A DSP is optimized for scientific calculations, specifically for fast Fourier transforms (FFT's), yet it provides more functionality and modularity than a traditional FFT chip. Not all DSPs provide the necessary I/O that is required for the large image sizes used in our application (a typical data set consists of four images at  $512 \times 512$  pixels and a 16 bit pixel depth). The Analog Devices TS-101 provides 1 GB/sec of I/O and 1.5 GFlops. It is this tight ratio of performance to bandwidth that sets apart the TigerSharc from other high end DSPs. At the time of purchase, the TS-101 was the highest performing DSP in the TigerSharc class.

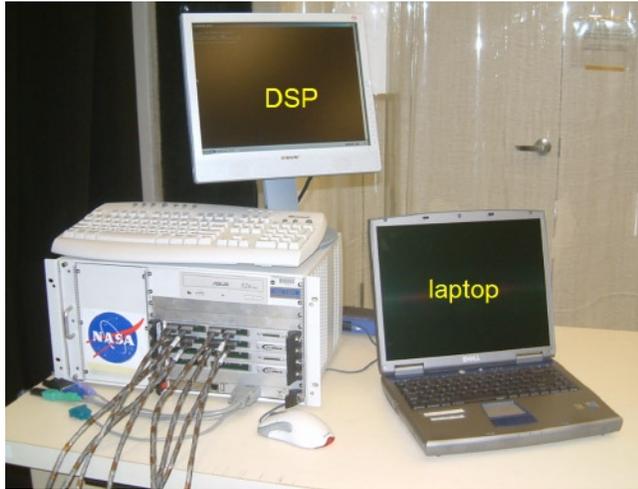
A block diagram of the 32 processor unit is shown in Figure 1 which consists of 4 cPCI boards with 8 DSP's/board. Figure 2 shows the unit built and tested next to a laptop control computer. The laptop computer is used for the data collection and calibration. The laptop then makes a function to the DSP processor using the software developed in this study. The DSP then returns an estimate of the optical system aberrations. Additional funding (outside the DDF) was obtained to procure

*Figure 1.  
Block Diagram of the  
32 Processor DSP Unit.*



32 additional processors, for a total of 64 DSP's, by utilizing PMC daughter cards available from Bittware, Inc. These are shown in Figure 3. Test and implementation of the additional processors will be discussed in a later report.

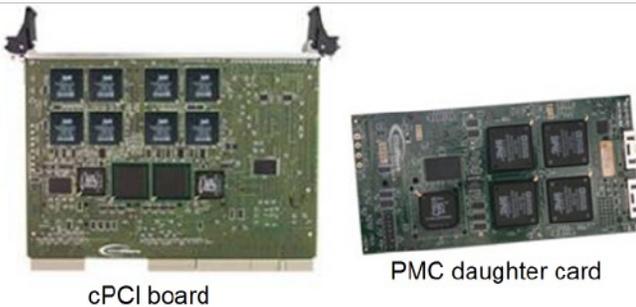
Figure 2. 32 Processor DSP Unit Built and Tested with a Laptop Control Computer.



Each DSP has two link ports connecting it to the other DSP's in its own cluster, signified by the red lines in Figure 4.

Additionally, each DSP has a third link port that can connect to any other DSP. In the development of this system, several architectures were examined that provided the most efficient use of the additional link port to perform the matrix transpose that is necessary for the 2-D FFT. The first architecture explored was a cube of 8 DSP's (see Figure 5). This architecture is ideal because the original system consisted of 32 DSP's and thus provides 8 DSP's per image. Yet, this architecture was unsatisfactory because of the inadequate size of internal memories and the large image sizes for our wavefront sensing algorithm.

Figure 3. cPCI boards with 8 DSP's/board and the PMC add-on daughter cards.



This can be seen from the simple calculation: each DSP has 6 Mbits of internal memory, 2 Mbits in program memory, 2 Mbits in data one, and 2 Mbits in data two. The baseline for the image size of the MGS is 512 x 512 pixels, which translates to 512 x 512 pixels x 64 bits / 8 DSP = 2.1 Mbits. This was too large to place in either of the data memories. The first architecture was designed to minimize the distance from any two DSP's (Figure 5). Each DSP was treated equally, and therefore, all link ports carried the same weight. Since each link port has a maximum capability of 250 MB/sec, this resulted in the network speed of 6 GB/sec (16 DSP \* 3 link ports \* 250 MB/sec / 2 [send & receive]).

Figure 4. LEFT DSP Link Ports (in Red)

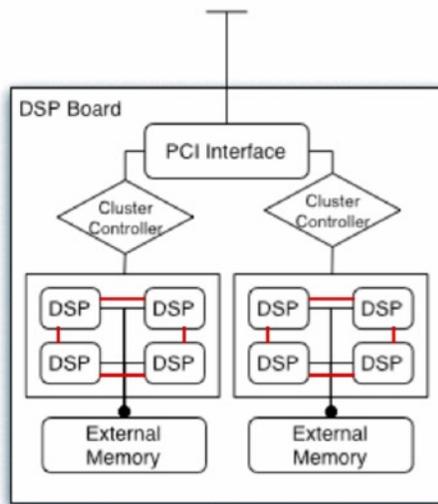
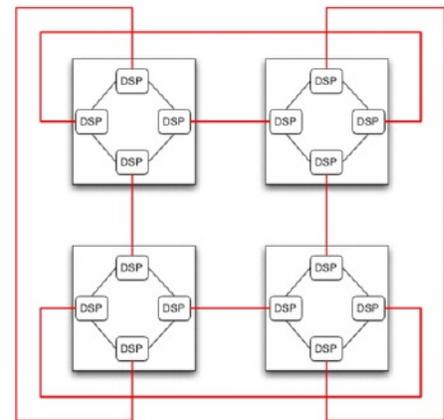
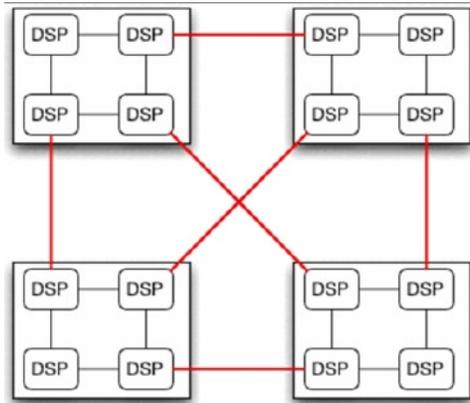


Figure 5. RIGHT Cube of 8 DSP's Architecture.



The second architecture studied (Figure 6) placed a greater emphasis upon the memory and data transfer hierarchy. Since a DSP can communicate to another DSP in its own cluster much faster than it can communicate to another DSP, it was decided to have each DSP act as a gateway to another cluster. A single DSP represents the entire cluster, and communicates with a single DSP that represents the second cluster. To provide inner communication within the cluster, a new protocol was utilized, the multi-processor memory space (MMS). The MMS simplifies small data transfers because there is little setup and handling compared to data transfer via link ports. The largest draw back to this approach is that it can not be scaled beyond 16 DSP's per sub-system without adding additional link ports.

*Figure 6. Second Architecture placing greater emphasis upon the memory and data transfer hierarchy.*



### **Publications and Conference Presentations:**

Results from this work have appeared in:

1. S. Smith, B. Dean, Tech Days, "WFS via High-Speed DSP." Huntsville Alabama, August 17–19, 2004.
2. B. Dean, S. Smith, Ed Lo "NASA – GSFC WFS&C Approach," presented at JPL JWST Workshop, 2004.
3. B. Dean, "Wavefront Sensing and Control for the DOT Testbed," Air-Force-Research-Labs, Albuquerque, NM, Feb, 2004
4. B. Dean, "Status on NASA Wavefront Sensing for Space Optics Control" to NASA Headquarters Core Capability Road-mapping Workshop for Large Aperture Telescopes," NASA GSFC, Dec. 1, 2004

### **Planned Future Work:**

Additional DDF funding will be requested in 2005 to make the DSP unit more compact and portable. Wavefront sensing architectures will also be developed to support data sets consisting of both a single image and 2 images, in addition to the 4 image case developed in this study. An additional goal will be to improve the processing time by another order of magnitude and therefore attain a full 3 orders of magnitude (factor of 1000) improvement in processing time over conventional computing architectures.

**Summary:**

Project's innovative features – this is the first documented implementation of high-speed wavefront sensing for space optics control using a cluster of DSP's. Through the use of a custom developed wavefront sensing architecture, our algorithms have been accelerated by two orders of magnitude over previous state-of-the-art. This technology enables space-optics control at previously unobtainable update rates to compensate for near-real time thermal/mechanical disturbances in the system.

Potential payoff to Goddard/NASA – NASA/GSFC has major activities in image-based wavefront sensing for space optics control. In addition to enabling a new class of missions with reduced opto-mechanical tolerances, this technology has the potential to make GSFC a lead Center and Government agency for testing and control of large light-weighted optical systems.

The criteria for success – The main criterion for success would have been achieving accelerated wavefront sensing - at least 1 order of magnitude over previous state-of-the-art.

Technical risk factors that might have, or that in fact have, prevented achieving success – It is well documented that FFT's can be accelerated using supercomputing resources. But in our application with multiple DSP's, significant data transfer rates must also be realized to match the FFT floating point performance required by our application. Given the initial success of the architecture developed here, we will continue this effort by scaling the architecture to additional DSP's and also repackaging the DSP's and power supply for increased portability.